INTEGRATED DYNAMIC MEMORY AND OPERATING METHOD

5   Cross-Reference to Related Application:

This application is a continuation-in-part of U.S. application

No. 10/206,299, filed July 26, 2002.

Background of the Invention:

10   Field of the Invention:

The invention relates to an integrated dynamic memory having a

memory cell array with memory cells for storing a charge

corresponding to an information bit. The invention further

relates to a method for operating an integrated memory of this

15   type.

Integrated memories, such as, for example, a dynamic random

access memory (DRAM) use capacitors for storing charge. The

charge state in the capacitor in each case represents an

20   information bit.

A DRAM chip contains a matrix of memory cells that are

arranged in rows and columns and that are addressed by word

lines and bit lines. Reading data from the memory cells or

25   writing data to the memory cells is realized by activating

suitable word lines and bit lines.

The charge stored in the capacitor decreases over time on account of recombination and leakage currents. Before the charge has decreased to an indeterminate level below a specific threshold value, the capacitor charge must be

5 refreshed. This operation is referred to as "refresh". For this reason, these memory cells are called dynamic RAM (DRAM), in contrast to static RAMs (SRAM), which do not need refreshing. A DRAM device which is operated synchronously to a clock signal is called a SDRAM (Synchronous Random Access

10 Memory).

The term retention time refers to that period of time for which a memory cell of a DRAM can retain the stored charge without falling below the threshold value. The refresh time,

15 specifically the time between two refresh operations, must therefore be equal to or shorter than the retention time so that data losses do not occur.

The refreshing of the storage capacitors is generally

20 controlled by an external module, for instance, the controller of a PC (Personal Computer) for all of the installed memory modules. A memory module includes several, e.g. 8 memory devices disposed on a common substrate which are operated in parallel. The module includes additional components. If the

25 memory devices of a memory module have different refresh times, the weakest memory device with the shortest refresh

time determines the refresh cycle of the module. The weakest

module determines the refresh cycle for all modules operated

in parallel. A refresh that is as infrequent as possible,

that is to say a long refresh time, is advantageous since

5   first the memory device and the module including several

parallel operated devices is blocked during the refresh and is

not available for other tasks, and second every refresh is

associated with a charge transport and thus a current

consumption. This has a disadvantageous effect particularly

10   in the case of portable devices, whose rechargeable-battery

operating time is critical.

A general problem in the case of the retention time of a

semiconductor memory is due to the fact that the retention

15   time is not an invariable constant, but rather can depend on

the ambient and operating temperature, and also on the age of

the memory device.

At the present time, this circumstance is taken into account

20   by assuming a maximum operating temperature, for example 95°C,

which is composed for instance of a maximum specified external

temperature of 70°C and an inherent heating proportion of

25°C. The memory device and the memory modules are then

tested at this temperature and memory cells which did not

25   satisfy the specification are replaced by redundant memory

cells, or the refresh time is set so conservatively at

delivery that the remaining memory cells have a retention time above the chosen refresh time up to the maximum temperature.

For a 128 Mbit memory device or component having 4096 rows
5 which are arranged in, for example, four banks, 64 ms, for example, is generally chosen as the refresh time for a four bank parallel refresh. The chip is tested at the maximum operating temperature at 64 ms and the weak cells are eliminated in a customary manner by redundancy repairs. After
10 a successful test of a memory device, it is then assumed that:

- the retention time was set correctly by fuses/trimmer;
- the retention is identical for volatile logic ones ("1") and logic zeros ("0");
15 - the defective cells have been eliminated by redundancy activation;
- the inherent chip heating does not increase in operation throughout the lifetime of the product;
- the retention susceptibility does not increase or vary with
20 respect to time, as in the case of the so-called "variable retention time";
- the actually tested temperature at which the retention time was determined is known precisely.

25 These expectations for the most part represent simplified assumptions which, when not completely applicable, are

compensated for, for example, by overtesting after production. Alternatively, these assumptions can lead to failures after a certain operating duration. This loss is unacceptable in particular in the case of high-reliability components, for

5 example, in mainframe computers, in power station control and the like.

Summary of the Invention:

It is accordingly an object of the invention to provide an

10 integrated dynamic memory which overcomes the above-mentioned disadvantages of the prior art apparatus of this general type.

In particular, it is an object of the invention to provide an integrated dynamic memory that when compared with conventional

15 dynamic memories, has a small current consumption and/or is available for random read/write accesses for the longest possible proportion of time.

With the foregoing and other objects in view there is

20 provided, in accordance with the invention, an integrated dynamic memory including a memory cell array having a regular cell area with regular memory cells, a first test cell area with first test cells, and a second test cell area with second test cells. The regular memory cells, the first test cells

25 and the second test cells are for storing a charge corresponding to an information bit. The integrated dynamic

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memory also includes: a control unit for refreshing charge contents of the regular memory cells with a first refresh time T_{ref}; a control unit for refreshing charge contents of the first test cells with a second refresh time T1, and for

5   refreshing charge contents of the second test cells with a third refresh time T2; and an evaluation unit for detecting memory cell defects in the first test cell area and in the second test cell area. The first refresh time T_{ref} is shorter than the second refresh time T1; and the second refresh time

10   T1 is shorter than the third refresh time T2.

The invention is thus based on the concept of functionally separating subareas of the memory cell array from the regular memory area and using them for monitoring and analyzing the

15   retention time that is presently required. In this case, the invention assumes that the cells used for the retention analysis have the same production-dictated retention quality as the regular memory cell array and the underlying statistics are not significantly impaired by the limited number of cells

20   used for the analysis.

Both assumptions are generally satisfied well, since the cell areas used for the retention analysis originate from the same memory cell array as the regular memory cells. Moreover,

25   after the redundancy activation, there are generally still sufficiently many redundant memory cells available which can

be utilized for the retention analysis with adequate
statistics.

Preferably, the evaluation unit has a device for altering the
5   refresh times T_{ref}, T1 and T2 on the basis of detected memory
cell defects. This makes it possible to adapt the refresh
time T_{ref} to instantaneous conditions depending on the result
of the memory tests carried out on the test cell areas, that
is to say to increase or decrease the refresh time T_{ref}. In
10 this case, operation is carried out with a longer refresh time
T1 in the first test cell area, and operation is carried out
with an even longer refresh time T2 in the second test cell
area.

15 If the evaluation of the memory test reveals that no memory
cell defects occurred even at the longer refresh times T1 and
T2, it can be concluded that the present operating conditions
according to the temperature and the age of the module also
permit the regular memory cells to be used with a longer
20 refresh time T_{ref} than presently set.

The refresh times T_{ref}, T1 and T2 are expediently chosen such
that the refresh time T1 is twice as long as T_{ref}, and the
refresh time T2 is twice as long as T1. The refresh time of
25 the first test cell area thus differs by the factor 2, and

that of the second test cell area by the factor 4, from the present setting for the regular memory areas.

This enables a reliable assessment of the appropriate refresh
5   rate: this is because if the first memory cell area runs with the refresh time T1 without any memory defects, it can be concluded that the present, shorter refresh time T_{ref} is in defect-free operation even with some safety margin. The first test cell area thus functions as a safety area whose
10 defectless or defective operation allows conclusions about the operating state of the regular memory area.

As described in detail further below, the defect assessments of the first and second test cell areas together can be used
15 not only to infer whether the regular memory cell area operates reliably, but also to determine the corrections that are necessary, if appropriate.

In a preferred refinement, the memory cell array of the
20 integrated memory is organized in row lines and column lines and the regular cell area, the first test cell area and the second test cell area in each case include a number of row lines.

25 In this case, the row lines of the first and/or second cell area may be arranged next to one another at the edge of the

regular memory cell area, or may be arranged between the row lines of the regular memory cell area. The first variant allows for simple access to the test cell areas arranged in a block-like manner, while in the second variant, it is ensured by the arrangement of the test cell rows between the regular memory cell rows in a particular manner that the test cell rows experience the same operating conditions and have the same physical properties as the regular memory cells. The retention behavior of the test cells is thus a true reflection of the retention behavior of the regular memory cells.

With the foregoing and other objects in view there is provided, in accordance with the invention, a method for operating the described integrated dynamic memory, which includes steps of: providing the integrated dynamic memory with a memory cell array having a regular cell area with regular memory cells, a first test cell area with first test cells, and a second test cell area with second test cells; providing the regular memory cells, the first test cells and the second test cells for storing a charge corresponding to an information bit; refreshing charge contents of the regular memory cells with a first refresh time T_{ref}; writing test patterns to the first test cells and to the second test cells; refreshing charge contents of the first test cells with a second refresh time T1, and refreshing charge contents of the second test cells with a third refresh time T2; providing the

first refresh time T_{ref} being shorter than the second refresh

time T2 and providing the second refresh time T2 being shorter

than the third refresh time T_{ref}; reading memory cell contents

of the first test cell area and the second test cell area and

5   detecting memory cell defects by comparing the memory cell

contents with the test patterns that were written to the first

test cells and to the second test cells; and checking the

first refresh time T_{ref} with regard to the memory cell defects

that were detected in the first test cell area and in the

10 second test cell area.

Preferably, in the method, after checking the first refresh

time T_{ref} with regard to detected memory cell defects:

15 - the first refresh time T_{ref} is lengthened, or is left

unchanged after reaching a maximum refresh time T_{max} if no

memory cell defects are detected in the first and second test

areas;

- the first refresh time T_{ref} is shortened, or is left

20 unchanged after reaching a minimum refresh time T_{min} if memory

cell defects are detected in both the first and the second

test areas; and

- otherwise the first refresh time T_{ref} is left unchanged.

25 In an expedient manner, after the first refresh time T_{ref} is

changed, the second and third refresh times of the test cell

areas are correspondingly adapted. In particular, in the event of lengthening the first refresh time T_{ref}, the second and third refresh times T1, T2 are lengthened, so that the first refresh time T_{ref} is shorter than the second refresh time

5   T1 and the second refresh time T1 is shorter than the third refresh time T2.

Equally, in the event of shortening the first refresh time T_{ref}, the second and third refresh times T1, T2 are shortened,

10   so that the first refresh time T_{ref} is shorter than the second refresh time T1 and the second refresh time T1 is shorter than the third refresh time T2.

The operating method can then proceed as described above, only

15   with changed refresh times. The refresh times can, of course, also be changed repeatedly one after the other or with a time interval, in order, for instance, to take account of further heating or cooling of the memory device or the memory module.

20   Preferably, the refresh times T_{ref}, T1 and T2 are doubled in the case of lengthening, and are halved in the case of shortening.

By way of example, the refresh times T_{ref}, T1 and T2 may assume

25   a value from the group 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, 1024 ms, 2048 ms and 4096 ms.

The minimum refresh time T_{min} is then 1 ms and the maximum refresh time T_{max} for the regular memory cells is 1024 ms. Of course, other values are also appropriate for the refresh times depending on the application and complexity of the

5   memory module and the memory device disposed on the module.

It is useful for the defect analysis if, in the event of memory cell defects being detected, the type of memory cell defects is ascertained, in particular whether only logic

10   zeros, only logic ones, or both have failed.

During the operation of a plurality of the integrated dynamic memory devices described, the following method steps are carried out:

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- for each of the integrated memory devices, in response to a request signal from an external controller, the refresh time T_{ref} thereof is determined and communicated to the controller;
- the controller determines the shortest of the refresh times;

20   and
- the shortest refresh time that has been determined is subsequently used for refreshing each of the plurality of memory devices.

25   In a refinement of this method, for each of the integrated memory devices, the refresh times T1 and T2 of the first and

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second test cells are continually determined and stored in registers of each of the devices. The refresh times T1, T2 of all of the memory devices are read out by an external controller, and the controller decides, on the basis of the

5   read out refresh times T1, T2, about outputting a request signal for determining the refresh times T_{ref} of the memory devices.

In the self-refresh mode, by contrast, each memory device can

10   execute its refresh mode without external control according to its own refresh time T_{ref}, even if this refresh time differs from the refresh time of the other installed memory devices.

The memory devices may be disposed on a substrate to form a

15   memory module. The memory devices on a module are operated in parallel.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

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Although the invention is illustrated and described herein as embodied in an integrated dynamic memory and operating method, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may

25   be made therein without departing from the spirit of the

invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 diagrammatically shows an exemplary embodiment of an inventive integrated dynamic memory; and

Fig. 2 diagrammatically shows a further exemplary embodiment of an inventive integrated dynamic memory.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown a block diagram of an exemplary embodiment of an inventive integrated dynamic memory, which is in this case a 128 Mbit DRAM 10. The memory device 10 contains a memory block 20 containing an array 22 of regular memory cells including 4096 regular row lines WL and 512 regular column lines BL in each of the four memory banks of the memory device.

In addition, the memory block 20 includes redundant memory cells, of which two cell areas 24, 26 are also available after the redundancy activation. In the exemplary embodiment, each of the cell areas 24, 26 contains forty-eight row lines WL,

5   but this number can vary depending on the number of cells required for the repair.

The memory cells of the regular memory area 22 serve for the standard writing and reading of data. The cell areas 24 and

10   26 function as test areas in which the memory cells are in each case refreshed with a rate that deviates from the regular memory area.

To that end, the memory block 20 is connected to a control

15   unit 30, which first refreshes the charge contents of the regular memory cells in a refresh cycle of T_{ref} = 64 ms. The control unit 30 also carries out, in a manner known per se, read/write accesses to the regular memory area 22, for example, the control unit 30 applies addresses and writes or

20   reads data from the memory block 20.

A further control unit 40 serves for addressing the test cell areas 24 and 26. The memory cells of the first test cell area 24 are first refreshed with a refresh time of $T1$ = 128 ms, and

25   those of the second test cell area 26 with a refresh time of $T2$ = 256 ms.

The control unit 40 then writes test patterns, specific sequences of logic 1s and 0s, to the test cell areas 24, 26, reads the stored patterns out again after the respective refresh time has elapsed, and compares them with the stored pattern. If no deviations are evident, the memory test is deemed to have been passed (PASS), and otherwise to have been failed (FAIL).

In the case of a failed test, for the defect analysis it is additionally ascertained whether the defects occurred only in those cells containing logic ones, whether the defects occurred only in those cells containing logic zeros, or whether both types of defect occur.

The result of the memory test is evaluated in an evaluation unit 50. In this case, four different test results are possible, which result in different further measures:

a) The memory test in the first test cell array 24 with T1 = 128 ms yields PASS and the memory test in the second test cell array 26 with T2 = 256 ms yields FAIL (for short: PASS/FAIL). In this case, the present refresh time T_{ref} = 64 ms is considered to be appropriate since the first test cell array with its longer (doubled) refresh time still does not produce any defects, but the refresh with the significantly longer

(quadrupled) refresh time in the second test cell array leads to memory defects. As a consequence, no change is made to the refresh time T_{ref} of the regular memory cells.

5   b) The memory test yields no defects in both test cell arrays with T1 = 128 ms and with T2 = 256 ms (PASS/PASS). In this case, the present refresh time T_{ref} = 64 ms can be lengthened to 128 ms since no memory defects occur at the latter time, nor at the even longer refresh time of the second test cell

10   array.

As a consequence, the refresh time T_{ref} is doubled to 128 ms. For further testing, the refresh times of the test cell arrays must also be adapted. T1 is doubled to 256 ms, and T2 to 512

15   ms, and the method is continued with the new refresh times. If only defect-free test results are again yielded, the refresh time can be increased further.

c) The memory test yields memory cell defects in both test

20   cell arrays with T1 = 128 ms and with T2 = 256 ms (FAIL/FAIL). In this case, the present refresh time T_{ref} = 64 ms is classified as too long.

As a consequence, the refresh time T_{ref} is halved to 32 ms.

25   For further testing, the refresh times of the test cell arrays must also be adapted. T1 is reduced to 64 ms, and T2 to 128

ms, and the method is continued with the new refresh times. If only defective test results are yielded again, the refresh time must be lowered further.

5 d) The memory test in the first test cell array 24 with T1 = 128 ms yields FAIL and the memory test in the second test cell array 26 with T2 = 256 ms yields pass (FAIL/PASS). This case should not occur in normal operation and is treated, if appropriate, as a unique isolated case. All of the refresh

10 times remain unchanged.

The regular memory cells thus always run with a refresh rate in the reliable range since, during operation in the settled state, even the test cell array with a refresh time twice as

15 long still does not yield any memory cell defects.

If the refresh time T_{ref} reaches a predetermined maximum value T_{max}, for example 1024 ms or 4096 ms, no further increase takes place, even if both test cell arrays run PASS. This allows

20 the use of a register with a predetermined width for controlling the refresh time.

Furthermore, no further reduction of T_{ref} takes place if a predetermined minimum value T_{min}, for example, 1 ms has been

25 reached, even if both test cell arrays yield FAIL. This takes

account of the fact that excessively short refresh times are
not expedient.

The test results and the measures provided are compiled in
abbreviated fashion in table 1.

Table 1:

Result 1 (T1)	Result 2 (T2)	Measure
PASS	FAIL	Normal case: no change
PASS	PASS	if $T_{ref} < T_{max}$: double T_{ref}, T1, T2
FAIL	FAIL	if $T_{ref} > T_{min}$: halve T_{ref}, T1, T2
FAIL	PASS	should not occur: no change

A further exemplary embodiment of an integrated memory is
illustrated in Fig. 2, where there is also a logical
assignment of the row lines of the memory block 120 to the
regular memory area and the first and second test cell areas.

However, in this embodiment, the row lines which are logically
associated with the different areas are not physically
arranged in a blockwise manner, but rather are intermixed.
Thus, the row lines 221-226 are part of the regular memory
area, the row lines 241, 242 are part of the first test cell

area, and the row lines 261, 262 are part of the second test cell area. Fig. 2 shows only a small number of row lines, for the sake of clarity. In practice, the number is significantly larger; by way of example, a 128 Mbit DRAM chip may include 4096 regular row lines and in each case 48 row lines in the two test cell areas. The arrangement scheme illustrated in Fig. 2 can also be maintained, in principle, with the higher number of rows.

An intermixed arrangement as in Fig. 2 has the additional advantage that the test row lines have the same average temperature as the regular row lines. Consequently, the retention behavior of the test cells represents a true reflection of the behavior of the regular memory cells.

In the case of an intermixed arrangement, it is necessary, of course, that the control unit 40 and the control unit 30 keep a record of the addresses of the test rows 241, 242, 261, 262 in the memory block 120 in order to avoid incorrect accesses.

In order to perform the retention analysis, in the exemplary embodiment, a register 32, 42, 44 of sufficiently high resolution is in each case used for the two test cell arrays and the regular memory cell array. The binary value of the register in each case specifies the refresh time of the relevant cell area in milliseconds. By way of example, the

register of the regular memory area 32 contains, after system

initialization, the binary value "0000001000000", for 64 ms,

the register 42 of the first test cell area contains the

binary value "0000010000000" for 128 ms, and the register 44

5   of the second test cell area contains the binary value

"0000100000000" for 256 ms. The twelve-bit-wide registers

allow refresh values up to 2^{12} (2^{12} = 4096 ms).

Depending on the result of the test cell analysis, all the

10   registers 32, 42, 44 are shifted by one bit toward the left or

right, which corresponds to a doubling or a halving of the

associated refresh time. In this case, before the bit shift,

a check is made to determine whether the maximum values have

been reached, that is to say, in the case of lengthening,

15   whether the refresh time T_{ref} is already 1024 ms, and in the

case of a reduction, whether it is already 1 ms. The refresh

times remain unchanged in both cases.

Overall, the memory device can thus react to altered external

20   influences by adapting the refresh time. The memory device is

thereby independent of operating and aging conditions.

During the operation of a plurality of such memory devices

which may be disposed within a memory module, the connected

25   controller has the possibility, in the so-called auto-refresh

operating mode, of accessing the individual refresh timer

values and of adapting its refresh rate to the worst (that is to say shortest) refresh time. To that end, the controller can send a request signal to the memory devices within the module which drive the individual values of T_{ref} from each of

5 the devices of the module. The shortest refresh time can then be determined, which is subsequently used for the refresh of each of the memory devices within the module.

The refresh times T1 and T2 are either determined once

10 individually in the sense of a measurement request, or are determined permanently independently of the refresh time T_{ref} and are stored in respective control registers.

In the so-called self-refresh operating mode, T1 and T2 must

15 be determined permanently, and each device of a group of devices or a memory module is able to follow its own refresh time $T_{ref,i}$.